ABSTRACT OF THE DISCLOSURE

An output driver circuit and current control technique to facilitate high-speed buses with low noise is used to interface with high-speed dynamic RAMs (DRAMs). The architecture includes the following components: an input isolation block (120), an analog voltage divider (104), an input comparator (125), a sampling latch (130), a current control counter (115), and a bitwise output driver (output driver A 107 and output driver B 111).